Amendments to the Specification:

Please replace paragraph beginning on page 4, line 6, with the following amended paragraph:

FIG. 2A shows a connection box used to connect the logic block 20 to the wiring segments 10 of FIG. 1. According to FIG. 2A, routing wires 301 of a wiring segment 10 are connected via track buffers 304 and a multiplexing circuit 60 controlled by selection signals ~~S0, S1.~~ S0 and S1, which are derived from a configuration information loaded to the FPGA and which may be stored in respective memory cells, e.g. Static Random Access Memory (SRAM) cells 302, to an input port of the logical block 20. Based on the combination of logical levels of the binary selection signals S0 and S1, one of the outputs of the track buffers 304 is connected to the input port of the logic block 20.

Please replace paragraph beginning on page 8, line 10, with the following amended paragraph:

The bias voltages can be generated on-chip by using the threshold drops of the PMOS and NMOS transistors. For high clock rates, this provides a stable reference, but for slow clock rates, a global on-chip reference generation circuitry which can be ~~control~~ controlled by the control circuit 50 can be provided.